

# Energy-Efficient Ternary Logic Processor Using CNTFETs for Advanced Nanotechnology Applications

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Published online: 31 March 2026

**Abstract** – The increasing demand for energy-efficient computing has driven research into novel logic architectures beyond traditional binary logic. This paper presents the design and implementation of an energy-efficient ternary logic processor using Carbon Nanotube Field-Effect Transistors (CNTFETs) for advanced nanotechnology applications. Ternary logic, which operates with three discrete states (0, 1, 2), offers higher computational density, reduced transistor count, and lower power consumption compared to conventional binary architectures. CNTFETs, with their superior electrical properties such as high carrier mobility, low sub-threshold swing, and excellent scalability, serve as an ideal candidate for implementing ternary logic circuits. The proposed ternary processor integrates ternary logic gates, arithmetic units, multiplexers, memory units, and control circuits, all optimized for low-power operation. Simulation results demonstrate significant improvements in energy efficiency, area reduction, and computational throughput compared to conventional CMOS-based binary processors. Additionally, the processor's architecture is tailored for emerging applications in artificial intelligence, cryptography, and IoT devices, where power efficiency and performance are critical. The findings of this study highlight the potential of CNTFET-based ternary computing as a promising alternative for next-generation low-power processors in nanotechnology-driven applications.

**Index Terms** – Ternary Logic Processor, CNTFET, Low-Power Computing, Nanotechnology, Energy-Efficient Architecture.

## I. INTRODUCTION

The rapid advancement of computing technologies has led to an increasing demand for energy-efficient and high-performance processors. Traditional binary logic-based architectures, which rely on 0 and 1 for computation, are reaching fundamental limitations in terms of power consumption, transistor density, and heat dissipation. As a result, researchers are exploring alternative computing paradigms to address these challenges, with ternary logic computing emerging as a promising solution. Ternary logic, which operates with three discrete states (0, 1, 2), offers several advantages over conventional binary logic, including higher computational density, reduced circuit complexity, and lower power consumption.

At the same time, Carbon Nanotube Field-Effect Transistors (CNTFETs) have gained significant attention as a next-generation alternative to conventional Complementary Metal-Oxide-Semiconductor (CMOS) technology. CNTFETs offer superior electrical properties such as high carrier mobility, better electrostatic control, reduced short-channel effects, and lower power dissipation, making them ideal for implementing ternary logic circuits. By combining ternary logic with CNTFET technology, it is possible to develop a highly efficient, low-power ternary logic processor that outperforms traditional binary processors in terms of energy efficiency and computational performance.

As transistor scaling approaches its physical limits, CMOS technology faces major challenges such as power leakage, heat dissipation, and increased complexity in interconnects. The aggressive downscaling of transistors has led to excessive static power dissipation, making power efficiency a critical concern for future computing systems. Furthermore, binary logic circuits require a large number of transistors to implement complex operations, which results in increased chip area, energy consumption, and fabrication costs. These challenges have driven research into alternative logic systems such as ternary computing and the use of emerging nanomaterials like CNTFETs.

Ternary computing, which extends the digital logic system from two states (0,1) to three states (0,1,2), presents several advantages. Since a single ternary digit (trit) carries more information than a binary digit (bit), fewer transistors are required for equivalent logic operations. This reduction in circuit complexity leads to lower power consumption by minimizing switching activity and interconnect overhead. Moreover, ternary logic enables higher computational density, allowing more data to be processed per unit area. It also improves signal processing and error correction capabilities in computing and communication systems while offering better compatibility with emerging quantum computing architectures.

CNTFETs provide an ideal device-level solution for implementing ternary logic due to their ability to control threshold voltage ( $V_{th}$ ) through CNT diameter and chirality. Unlike conventional MOSFETs, which require additional circuit components to implement multi-valued logic, CNTFETs can be designed to operate in distinct voltage levels, making them highly suitable for ternary logic gates. The ability to adjust threshold voltage enables efficient implementation of ternary logic gates such as T-NOT, T-AND, T-OR, and T-XOR without requiring excessive circuit complexity. Additionally, CNTFETs exhibit lower leakage power due to their superior subthreshold characteristics, making them energy-efficient and ideal for low-power computing applications. Furthermore, their scalability for nanotechnology applications ensures compatibility with ultra-scaled technology nodes, making them suitable for future-generation processors.

The proposed ternary logic processor is designed using CNTFET-based ternary logic gates, arithmetic circuits, memory units, and control logic. The architecture leverages ternary arithmetic operations such as addition, multiplication, and subtraction to perform computations more efficiently than traditional binary processors. The key components of the processor include ternary logic gates, ternary arithmetic units, memory units, and a control unit optimized for low-power operation. The ternary arithmetic unit comprises ternary adders, multipliers, and logic units designed for high-speed calculations. The memory unit incorporates CNTFET-based ternary SRAM and DRAM for efficient data storage, while the control logic follows a ternary instruction set architecture (ISA) tailored for energy-efficient computing.

A CNTFET-based ternary logic processor has the potential to revolutionize computing in several fields. In artificial intelligence and machine learning applications, ternary logic enables efficient neural network computations, reducing energy consumption in AI hardware accelerators. In cryptography and security, ternary logic provides enhanced security by improving data encryption and decryption efficiency. For the Internet of Things (IoT), energy-efficient ternary processors can power ultra-low-power IoT devices, extending battery life and reducing operational costs. Additionally, ternary logic can contribute to neuromorphic computing by enabling brain-inspired architectures for real-time signal processing. Since ternary logic aligns well with qubits' multiple states in quantum computing, it can also serve as an intermediate step toward hybrid quantum-classical computing architectures.

This research aims to design, implement, and evaluate a CNTFET-based ternary logic processor for next-generation computing. The main contributions of this work include the design of novel CNTFET-based ternary logic gates and arithmetic circuits, the implementation of a low-power ternary logic processor with optimized energy efficiency, and a performance analysis comparing the

proposed ternary processor with traditional binary CMOS processors. The study evaluates power consumption, computational efficiency, and speed in various applications, demonstrating the advantages of ternary logic for modern computing needs.

The combination of ternary logic and CNTFET technology offers a viable path toward energy-efficient, high-performance computing. By leveraging multi-valued logic and nanotechnology, the proposed ternary logic processor addresses the power and scalability challenges of conventional CMOS binary processors. This study aims to pave the way for next-generation low-power computing architectures, unlocking new possibilities for AI, IoT, quantum computing, and beyond.

## II. RELATED WORK

"Design and Performance Comparison of CNTFET-Based Binary and Ternary Logic Inverter and Decoder With 32 nm CMOS Technology" by Mayuri Khandelwal and Neha Sharan (2017): This paper compares ternary and binary logic gate designs using CMOS and CNTFET technologies. The study demonstrates that CNTFET-based ternary logic gates exhibit reduced propagation delay and enhanced performance over their CMOS counterparts [1].

"Energy Efficient Tri-State CNFET Ternary Logic Gates" by Sepher Tabrizchi, Fazel Sharifi, and Abdel-Hameed A. Badawy (2018): This study introduces a novel method for designing ternary logic circuits using CNTFETs, leveraging their unique properties like adjustable threshold voltages. The proposed designs implement logic functions and their complements via a control signal and include a high impedance state to conserve power when inactive. A 2-digit adder-subtractor circuit is also presented, with simulations confirming correct operation under various conditions [3-5].

"CNTFET-Based Ternary Address Decoder Design" by Rawan Mohammed, Mohammed E. Fouda, Ihsen Alouani, Lobna A. Said, and Ahmed G. Radwan (2022): This paper presents three different designs for ternary address decoders based on CNTFETs, exploring new paradigms for scalable computing systems beyond Moore's law [6-7]. The study compares the proposed designs with binary address decoders in terms of power and delay under varying supply voltage and temperature conditions, highlighting the potential of MVL systems in enhancing data density and processing efficiency.

## III. PROPOSED METHOD

The proposed system introduces an energy-efficient ternary logic processor based on Carbon Nanotube Field-Effect Transistors (CNTFETs) to overcome the limitations of traditional binary and ternary logic implementations [8]. The system leverages the unique characteristics of CNTFETs to

enhance computational efficiency, reduce power consumption, and improve scalability for next-generation nanotechnology-based computing systems. Its scalability

makes it suitable for integration into emerging technologies such as AI, IoT, and advanced nanoelectronic systems [9].

Table 1 summarizes all major existing ternary and binary implementation approaches.

Method	Technology Used	Advantages	Limitations	Scalability
CMOS-Based Ternary Logic	Multiple Threshold CMOS	Compatible with existing fabrication	High leakage power, complex voltage generation	Limited beyond deep submicron nodes
Resistor-Transistor Logic (RTL)	Resistors + MOSFET	Simple conceptual design	High static power dissipation	Poor scalability
Capacitor-Based Ternary Circuits	Charge storage circuits	Intermediate voltage generation	Slow switching, unstable noise margins	Limited
CNTFET-Based Logic Gates	Carbon Nanotube FET	Low power, adjustable threshold voltage	Fabrication challenges	High potential for nanoelectronics
FPGA-Based MVL Systems	Reconfigurable logic blocks	Flexible architecture	Hardware overhead, inefficient voltage encoding	Moderate

### 3.1 Key Features of the Proposed System

The proposed system introduces a CNTFET-based ternary logic processor that operates on three logic levels (0, 1, and 2), reducing the number of gates and interconnections compared to conventional binary CMOS systems. By adjusting carbon nanotube diameters, CNTFETs provide multiple threshold voltages ( $V_{th}$ ), making them highly suitable for implementing stable multi-valued logic. Optimized ternary gates such as T-inverter, T-NAND, T-NOR, and T-XOR are designed to minimize transistor count, circuit complexity, and power consumption while improving switching performance [10].

The architecture integrates a ternary Arithmetic and Logic Unit (T-ALU) capable of performing ternary addition, subtraction, multiplication, and logical operations efficiently. Due to the high carrier mobility and low leakage characteristics of CNTFETs, the T-ALU achieves reduced propagation delay and lower energy dissipation compared to CMOS-based designs. Additionally, a ternary register and memory unit enhances data density by storing multi-valued information, improving storage utilization and potentially reducing access time.

Overall, the proposed processor offers reduced power consumption, higher computational efficiency, and a compact footprint due to fewer required transistors and interconnects.

The CNTFET-based ternary logic approach thus provides a promising pathway toward low-power, high-performance next-generation computing architectures.

### 3.2 Ternary Logic Implementation Using CNTFETs

Carbon Nano-tube Field-Effect Transistors (CNTFETs) are highly suitable for implementing ternary logic due to their capability to provide adjustable threshold voltages ( $V_{th}$ ). Unlike conventional CMOS devices, the threshold voltage of a CNTFET can be precisely tuned by varying the diameter of the carbon nanotube, enabling stable realization of multiple switching levels within a single device technology. This inherent property simplifies the implementation of multi-valued logic and ensures reliable discrimination among three voltage states in ternary systems.

In a CNTFET-based ternary logic architecture, three distinct voltage levels are typically defined as 0 V (Logic 0),  $V_{dd}/2$  (Logic 1), and  $V_{dd}$  (Logic 2). By designing devices with different threshold voltages, the circuit can accurately detect and process these intermediate states without additional complex biasing networks. Fundamental ternary building blocks such as the ternary inverter (T-INV), ternary NAND (T-NAND), ternary NOR (T-NOR), ternary XOR (T-XOR), Multiplexers, and decoders can thus be efficiently realized with reduced transistor count and improved switching performance[11-14].

The use of CNTFET-based ternary logic significantly reduces circuit complexity and interconnection overhead compared to binary implementations. Fewer transistors per function lead to lower power consumption and reduced area, while the ability to encode more information per signal enhances data density in arithmetic and memory circuits. Consequently, CNTFET-enabled ternary processors provide a scalable and energy-efficient solution for next-generation nanoelectronic systems, particularly in emerging domains such as AI, IoT, and advanced computing architectures.

### 3.3 Ternary NOT (TNOT) and Ternary AND (TAND) Gates Using CNTFETs

The TNOT (Ternary NOT) gate is a fundamental unary gate that inverts a ternary input (0, 1, 2) into its complement. Unlike binary NOT, which has only two states, the TNOT gate must map each input to a distinct output in a three-valued logic system.

Table 2: Truth table for TNOT Gate

Input (X)	Output (TNOT X)
0	2
1	1
2	0

The CNTFET-based implementation of the ternary NOT (TNOT) gate utilizes multiple threshold voltages ( $V_{th1}$ ,  $V_{th2}$ ) to accurately distinguish and switch among the three logic levels (0, 1, 2). By carefully designing the pull-up and pull-down networks, the circuit assigns the appropriate output voltage corresponding to each input state. The inherent multi-threshold capability of CNTFETs enables compact realization of the TNOT function with reduced device count, low power dissipation, and fast switching characteristics, making it highly efficient for multi-valued logic applications.

Table 3: Truth table for Ternary AND Gate

A	B	Output (A^B)
0	0	0
0	1	0
0	2	0
1	0	0
1	1	1
1	2	1
2	0	0
2	1	1
2	2	2

The ternary AND (TAND) gate extends the binary AND operation to a three-level logic system. Its operation follows the rule that the presence of logic 0 at any input forces the output to 0, while logic level 2 is produced only when both inputs are at level 2; intermediate combinations generate corresponding lower-level outputs. In CNTFET-based implementations, variable threshold devices and optimized

series-parallel configurations are employed to achieve correct ternary switching behavior. This approach reduces transistor count compared to equivalent CMOS-based ternary realizations and enhances power efficiency and data density.

Overall, CNTFET-based TNOT and TAND gates offer significant advantages, including reduced transistor count, lower leakage power, improved switching speed, and strong scalability for nanoscale integration. These fundamental ternary logic gates serve as essential building blocks for higher-level components such as ternary arithmetic logic units (T-ALUs), multiplexers, and memory circuits. Consequently, they form a critical foundation for the development of efficient CNTFET-based ternary logic processors targeting next-generation low-power and high-performance computing systems.

## IV. RESULTS AND DISCUSSIONS

The proposed CNTFET-based ternary logic processor was designed and simulated to evaluate its performance in terms of power consumption, area efficiency, and computational performance. Simulation results indicate that ternary logic circuits require fewer transistors compared to conventional binary CMOS circuits because each logic element can represent three states (0, 1, 2). As a result, the overall processor architecture achieves significant area reduction and improved circuit density, which is beneficial for nanoscale integrated circuits.

The use of Carbon Nanotube Field-Effect Transistors (CNTFETs) further enhances performance due to their high carrier mobility, low leakage current, and excellent scalability. These properties contribute to lower switching energy and reduced static power consumption, leading to improved energy efficiency. Compared to traditional CMOS-based processors, the CNTFET-based ternary processor demonstrates reduced power dissipation and faster switching speed, making it suitable for low-power computing environments.

The implemented ternary components such as ternary logic gates, multiplexers, arithmetic units, and memory modules function correctly under the designed architecture. Simulation results confirm that the processor can efficiently perform arithmetic and logic operations while maintaining stable voltage levels for ternary states. The reduced transistor count also simplifies circuit design and minimizes interconnection complexity.

Table 4: Comprehensive Comparison of Binary (CMOS) and Ternary (CNTFET) ALU Architectures[15]

Category	Parameter / Operation	Binary Logic (CMOS)	Ternary Logic (CNTFET)	Improvement / Reduction
Logic	Number of Logic Levels	2 (0,1)	3 (0,1,2)	Higher data representation per

Characteristics				trit
Characteristics	Transistors per Gate	High	33–50% Less	30–50% Reduction
	Energy per Operation	Higher (more switching)	Lower (fewer transitions)	Reduced dynamic power
	Interconnect Power	High	Lower (fewer wires)	Reduced wiring overhead
	Processing Capability	Binary data only	More information per trit	Increased data density
Power Analysis	Static Power (mW)	3.2 mW	2.1 mW	~34% Reduction
	Dynamic Power (mW)	15.7 mW	9.5 mW	~39% Reduction
	Total Power (mW)	18.9 mW	11.6 mW	~38% Reduction
Transistor Count	Full Adder	28	16	42% Reduction
	Multiplier	64	40	38% Reduction
	XOR Gate	8	4	50% Reduction
	AND Gate	6	3	50% Reduction
Propagation Delay (ns)	Addition	2.3 ns	1.2 ns	47% Faster
	Multiplication	5.6 ns	3.4 ns	39% Faster
	XOR Operation	1.8 ns	1.0 ns	44% Faster
	AND Operation	1.2 ns	0.7 ns	42% Faster

Furthermore, the processor architecture shows strong potential for emerging applications such as artificial intelligence, cryptographic systems, and Internet of Things (IoT) devices, where power efficiency and compact hardware design are essential. Overall, the results demonstrate that CNTFET-based ternary processors provide a promising alternative to conventional binary CMOS processors, offering improved energy efficiency, reduced chip area, and enhanced computational capability for next-generation nanoelectronic systems.

## V. CONCLUSION

The development of a CNTFET-based ternary logic processor presents a significant advancement in the field of low-power,

high-efficiency computing. By leveraging the multi-valued nature of ternary logic and the superior electrical properties of CNTFETs, the proposed architecture achieves reduced power consumption, lower transistor count, and faster computation speeds compared to traditional binary CMOS-based processors. The results demonstrate that ternary logic is a viable alternative for next-generation computing, particularly in applications such as AI, IoT, and quantum computing.

However, challenges remain in terms of scalable CNTFET fabrication, integration with existing digital architectures, and the development of ternary memory and software support. Future research should focus on optimizing these aspects to fully unlock the potential of ternary computing. Overall, this study paves the way for the adoption of ternary logic in

nanotechnology-based processors, offering a more efficient and sustainable approach to computing in the era of rapidly growing data and energy demands

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*Funding Declaration*

The authors declare that no funds, grants, or other forms of financial support were received from any organization or institution for the conduct of this research.

